IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application of

Applicant	: David L. Chapek
Serial No.	: 09/605,293
Filed	: June 28, 2000
Title	: SEMICONDUCTOR DEVICES INCLUDING A LAYER OF POLYCRYSTALLINE SILICON HAVING A SMOOTH MORPHOLOGY
Docket No.	: MIO 0037 VA/40509.118
Examiner	: Kim, Jay C
Art Unit	: 2815
Confirmation No.	: 5927

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

BRIEF ON APPEAL

This is an appeal from the Office Action mailed September 18, 2008, rejecting claims 9-12 and 14, all of the claims in the application. A Notice of Appeal was timely filed on November 17, 2008 with the accompanying fee. An authorization to charge our credit card in the amount of $540 accompanies this Brief in accordance with 37 CFR §41.20(b)(2).

Real Party in Interest

The real party in interest in this application is Micron Technology, Inc., by an assignment from the named inventors recorded in the files of the U.S. Patent and Trademark Office at Reel 9159, Frame 0921.

Related Appeals and Interferences

This application was the subject of a prior appeal filed June 3, 2004. Following the filing of the appeal, prosecution was re-opened (see Office Action mailed August 26, 2004); therefore no decision was rendered by the Board. A second appeal was filed on

July 19, 2005, and prosecution was again re-opened (see Office Action mailed October 4, 2005). A third appeal was filed on December 19, 2005 (Appeal No. 2006-2669), and a decision was rendered in that appeal on September 21, 2007. A copy of the decision is attached in the Related Proceedings Appendix.

Status of Claims

Claims 9-12 and 14 are pending in this application and are before the Board for consideration on appeal. Claims 1-8 and 13 were previously cancelled. A copy of the appealed claims is found in the Appendix attached to this brief.

Status of Amendments

No amendments to the claims were filed after final rejection. All previous amendments have been entered.

Summary of Claimed Subject Matter

The following is a concise explanation of the subject matter defined in each of the independent claims and each of the dependent claims argued separately. Reference to the drawing figures and specifically depicted embodiments of the invention are for the convenience of the Board and not to be interpreted as limitations on the claims.

Claim 9

The subject matter of independent claim 9 is shown by way of example in the embodiment illustrated in Fig. 1 and described at pages 7-10 of the specification. A layer 14 of silicon dioxide 16 is formed on a semiconductor substrate 12. After the layer 14 is doped with hydrogen ions deposited by a plasma source ion implantation process, a layer 18 of polycrystalline silicon 20 having a smooth morphology is formed on the layer 14 of silicon dioxide. The layer of silicon dioxide has reduced sputtered metal contaminants in comparison with a layer of silicon dioxide doped with ions deposited by a Kauffman ion implantation process (see the specification at page 10, lines 6-13).

Claim 10

The subject matter of independent claim 10 is shown by way of example in the embodiment illustrated in Fig. 2 and described in the specification at pages 10-11. A field effect transistor is provided which comprises a layer of silicon dioxide formed on a semiconductor substrate 52 (page 10, lines 21-24). The surface of the substrate 52 includes hydrogen ions implanted by plasma source ion implantation (page 11, lines 14-16) such that the layer of silicon dioxide has reduced sputtered metal contaminants in comparison with a layer of silicon dioxide doped with ions deposited by a Kauffman ion implantation process. The substrate further includes a layer of polycrystalline silicon 66 on the layer of silicon dioxide, a gate oxide 54, a source 56 and drain 58, and a gate electrode 70 (page 11, lines 12-18).

Claim 11

The subject matter of independent claim 11 is shown by way of example in the embodiment illustrated in Fig. 3 and described at page 12, lines 4-16. A memory array 100 is provided including a silicon dioxide layer formed on a semiconductor substrate and implanted with hydrogen ions by plasma source ion implantation such that the layer of silicon dioxide has reduced sputtered metal contaminants in comparison with a layer of silicon dioxide doped with ions deposited by a Kauffman ion implantation process (page 10, lines 6-13). A layer of polycrystalline silicon is formed over the silicon dioxide layer having a smooth morphology. The memory array further includes a plurality of memory cells 102 arranged in rows and columns, each of which comprise at least one field effect transistor 50, a gate oxide for each of the field effect transistors, a source and drain for each of the field effect transistors, and a gate electrode for each of the field effect transistors (page 12, lines 4-16).

Claim 12

The subject matter of independent claim 12 is shown by way of example in the embodiment illustrated in Fig. 4 and described at page 12, lines 17-24. A

semiconductor wafer W is provided including a layer of silicon dioxide formed on a semiconductor substrate 52 and implanted with hydrogen ions by plasma source ion implantation such that the layer of silicon dioxide has reduced sputtered metal contaminants in comparison with a layer of silicon dioxide doped with ions deposited by a Kauffman ion implantation process (page 10, lines 6-13). A layer of polycrystalline silicon is formed over the silicon dioxide layer and has a smooth morphology. The semiconductor wafer W is divided into a plurality of die and comprises a repeating series of gate oxides formed on the semiconductor substrate, a repeating series of sources and drains for at least one field effect transistor formed on each of the plurality of die, and a repeating series of gate electrodes for the field effect transistor formed on each of the plurality of die.

Claim 14

The subject matter of independent claim 14 is shown by way of example in Fig. 5 and described at pages 13-14. A thin film transistor is provided in which a semiconductor substrate 202 formed from a layer of silicon dioxide, glass or quartz is implanted with hydrogen ions by plasma source ion implantation, where the substrate has reduced sputtered metal contaminants in comparison with a substrate doped with ions deposited by a Kauffman ion implantation process. A layer of polycrystalline silicon 206 is formed over at least a portion of the silicon dioxide layer, where the polycrystalline silicon layer has a smooth morphology. The thin film transistor 200 includes a layer of insulating material formed on at least a portion of the polycrystalline silicon, a gate oxide formed from the layer of insulating material, a source and drain region formed in the polycrystalline silicon layer, and a gate electrode formed on the layer of insulating material (page 13, lines 2-9).

Grounds of Rejection to be Reviewed on Appeal

The grounds of rejection for review on appeal are:

1) Claims 9-12 and 14 are rejected under 35 USC §112, second paragraph, as being indefinite.

2) Claim 9 is rejected under 35 USC §102(a) as being anticipated by "Applicant's admitted prior art."

3) Claims 9 and 10 are rejected under 35 USC §102(b) as being anticipated by Zhang et al (US 5,946,585), as evidenced by Nakanishi et al (US 6,265,247).

4) Claim 14 is rejected under 35 USC §102(b) as being anticipated by Shufflebotham (US 5,711,998).

5) Claims 10-12 are rejected under 35 USC §103(a) as being unpatentable over Burns et al. (Principles of Electronic Circuits, pp. 380-381) in view of "Applicant's admitted prior art."

6) Claim 14 is rejected under 35 USC §103(a) as being unpatentable over Murata et al. (U.S. 5,576,229) in view of "Applicant's admitted prior art."

ARGUMENT

Rejection under 35 USC. §112, second paragraph

Claim 9

The Examiner maintained in the final Office Action that the limitation "has reduced sputtered metal contaminants in comparison with a layer of silicon dioxide doped with ions deposited by a Kauffman ion implantation process" renders the claim indefinite as "the ordinary artisan would not know what level of metal contaminants is required to meet the limitation." The Examiner further asserted that whether or not the metal contaminants are "sputtered" metal contaminants "make no structural difference in the product," and that there is no way to determine if metal contaminants in the final product came from a Kauffman ion implantation process or another source. Applicant disagrees with the Examiner's reasoning. The claim simply recites that the layer of silicon dioxide formed on the semiconductor substrate is doped with hydrogen ions. The manner in which the layer is doped results in a silicon dioxide layer having reduced, i.e., fewer, metal contaminants than if the hydrogen ions were implanted using a Kauffman ion implantation technique. There is no need to quantify or to determine the amount of metal contaminants as the claim language clearly conveys that the claimed silicon dioxide layer has fewer metal contaminants than a layer doped utilizing the Kauffman ion implantation technique.

While the Examiner asserted at page 11 of the office action that one skilled in the art cannot determine whether the amount of metal contaminants is smaller than that produced by a Kauffman ion implantation process without measuring the amount, such does not render the claim indefinite. Kauffman ion implantation is a known technique that produces known and measurable levels of metal contamination on the surfaces of target objects. The claimed doped silicon dioxide layer simply has a reduced level of metal contamination when compared with the known Kauffman ion technique. Applicant

submits that the scope of the claimed subject matter would be understood by one skilled in the art, i.e., one skilled in the art would know what is meant by "reduced sputtered metal contaminants in comparison with a semiconductor substrate doped with ions deposited by a Kauffman ion implantation process."

Applicant's position is supported by the Board Decision on Appeal decided in this application on September 21, 2007, in which the Board stated that the applicant's specification describes a process that produces a semiconductor device in which the possibility of metal contamination is reduced when compared to the prior art Kauffman ion source implantation technique. See the Board's statement at pages 14-15 of the decision, appended to the Related Proceedings Appendix in this Brief.

Claim 9 is in compliance with §112, second paragraph.

Claim 10

As understood, the basis for this rejection is the Examiner's objection to the same language found in claim 9. Claim 10 is in compliance with §112, second paragraph, for the same reasons stated above with regard to claim 9.

Claim 11

As understood, the basis for this rejection is the Examiner's objection to the same language found in claim 9. Claim 11 is believed to be in compliance with §112, second paragraph, for the same reasons stated above with regard to claim 9.

Claim 12

As understood, the basis for this rejection is the Examiner's objection to the same language found in claim 9. Claim 11 is believed to be in compliance with §112, second paragraph, for the same reasons stated above with regard to claim 9.

Claim 14

With respect to the recited claim language, "the surface of said semiconductor substrate having hydrogen ions implanted therein … has reduced sputtered metal contaminants in comparison with a semiconductor substrate doped with ions deposited by a Kauffman ion implantation process," applicant submits that this language is in compliance with 112, second paragraph, for the same reasons stated above with respect to claim 9.

Further, the Examiner maintained at page 3 of the final office action that the claim language "a semiconductor substrate formed from a material selected from the group consisting of silicon dioxide, quartz and glass" renders the claim indefinite, asserting that it is unclear how the substrate can be a semiconductor substrate when it is made of an insulating material. Applicant previously pointed out that the recited materials are commonly used as semiconductor substrates, i.e., as described and explained in the specification at page 7, lines 18-27, such materials are commonly used to form the substrate on which a semiconductor device is fabricated. Further, the recited materials find clear support in the specification as originally filed (see page 6, lines 5-6 and page 7, lines 25-27). The term "semiconductor substrate" has been defined and explained in the specification such that a person skilled in the art would immediately understand its meaning in the context of the present application and claims.

At page 11 of the final office action, the Examiner asserted that applicant does not specifically claim a substrate on which a semiconductor is formed, but claims a semiconductor substrate, "which suggests that the substrate comprises [a] semiconductor." Applicant disagrees. The specification clearly defines a semiconductor substrate as a substrate which is part of a semiconductor device, i.e., a substrate which forms a semiconductor device. See, e.g., page 7, lines 18-22

Applicant submits that claim 14 is definite and in compliance with §112, second paragraph.

Rejection under 35 USC §102(a) as being anticipated by "Applicant's admitted prior art" (APA)

A prior art reference anticipates the subject matter of a claim when the reference discloses every feature of the claimed invention, either explicitly or inherently (see *Hazani v. Int'l Trade Comm'n*, 126 F.3d 1473, 1477, 44 USPQ2d 1358, 1361 (Fed. Cir. 1997) and *RCA Corp. v. Applied Digital Data Systems, Inc.*, 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir. 1984)). Rejections under 35 USC §102 are proper only when the claimed subject matter *is* identically disclosed or described in the prior art. Thus, for a rejection under 35 USC §102 to be proper, the prior art reference must clearly and unequivocally disclose the claimed device, or direct those skilled in the art to the claimed device without *any* need for picking, choosing, and combining various disclosures not directly related to each other by the teachings of the cited reference. *In re Arkley*, 172 USPQ 524 (CCPA 1972).

Claim 9

The Examiner acknowledged in the final office action at page 4 that the "APA" does not explicitly state that the layer of silicon dioxide disclosed therein "has reduced sputtered metal contaminants in comparison with a layer of silicon dioxide doped with ions deposited by a Kauffman ion implantation process," but asserts that "this limitation is inherent." The Examiner further asserts that the "level of metal contaminants imparted by the Kauffman ion implantation process of the "APA" can be considered 'reduced' compared to an arbitrary ion implantation process conducted at a higher energy and/or for a longer time." Applicant previously pointed out that claim 9 does not refer to an "arbitrary" implantation process, but refers specifically to the comparison of a silicon dioxide layer deposited with ions by a plasma ion source implantation process

with that of the (same) silicon dioxide layer deposited with ions by a Kauffman ion implantation process. Hence, the claimed comparison cannot be inherent in the "APA." Further, as the "APA" *describes* a Kauffman ion implantation process, that process cannot result in reduced sputtered metal contaminants in comparison to itself.

At page 11 of the final office action, the Examiner asserted that because applicant does not claim specific operating parameters of a Kauffman ion implantation process, "one Kauffman ion implantation process would inherently produce reduced sputtered metal contaminants in comparison with another Kauffman ion implantation process." Such an assertion is speculative and ignores the explicit language of the claim. The Examiner further reasoned that he had provided a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art. Applicant strongly disagrees. The Examiner's speculation provides no factual basis for his reasoning, i.e., the Examiner has provided no evidence that using a Kauffman ion implantation process in one instance would provide reduced sputtered metal contaminants when using the same process in another instance. And, such speculation ignores that the claim recites a hydrogen ion doped silicon dioxide layer, the ions deposited by a plasma source ion implantation process.

Claim 9 is not anticipated by the "APA."

<u>Rejection under 35 USC §102(b) as anticipated by Zhang et al (US 5,946,585), as evidenced by Nakanishi et al (US 6,265,247)</u>

<u>Claim 9</u>

Applicant notes that the Examiner has given no patentable weight to the claimed limitation "having been doped with hydrogen ions deposited by a plasma source ion implantation process," asserting that this is a product-by-process limitation which does not structurally distinguish the claimed invention over the prior art. Applicant previously pointed out that the method by which the layer has been formed directly affects the composition of the final product with regard to the level of metal contaminants in the

silicon dioxide layer. A silicon dioxide layer with no metal contaminants or having a reduced level of metal contaminants is clearly <u>compositionally</u> different than a silicon dioxide layer having greater levels of metal contamination. And, as taught in the specification, such a <u>compositional</u> difference affects the performance of the device.

At page 12 of the final office action, the Examiner responded by asserting that applicant has not provided evidence that the plasma CVD process of Zhang et al. "will always produce greater level of metal contamination in comparison with any Kauffman ion implantation process." However, applicant is not required to provide such evidence as the Examiner has not established that claim 9 is anticipated by Zhang et al. Zhang et al. do not teach a layer of silicon dioxide the surface of which is doped with hydrogen ions deposited by a plasma source implantation process as claimed, so it is irrelevant whether or not Zhang's plasma CVD process would produce greater or lesser levels of metal contamination than a Kauffman ion implantation process. Zhang simply does not teach, expressly or inherently, a semiconductor device having a layer of silicon dioxide thereon, with the surface of that layer doped with hydrogen ions.

The Examiner further concluded at page 6 that "since no Kauffman ion implantation process is conducted during the manufacturing of the device of Zhang, it is inherent that the oxide layer has reduced sputtered metal contaminants in comparison with a silicon dioxide doped with ions deposited by a Kauffman ion implantation process." Again, the Examiner's logic is flawed. There is no teaching or suggestion in either Zhang et al. or Nakanishi et al. of a layer of silicon dioxide the surface of which is doped with hydrogen ions deposited by a plasma source implantation process. Rather, Zhang et al. teach formation of a silicon oxynitride film by plasma CVD (coll. 4, lines 44-45).

The Examiner has further concluded that the silicon oxynitride layer 104 of Zhang et al. would inherently contain some hydrogen and opines that the factual basis for such a conclusion is provided by Nakanashi, who "clearly disclose a hydrogen ion concentration of a silicon oxide film formed by plasma CVD." However, what Nakanishi et al. actually teach at column 2, lines 30-34, is that the hydrogen ion concentration of

silicon *nitride* films formed by plasma CVD is higher than the hydrogen ion concentration of silicon *oxide* films formed by the same plasma CVD method.

This does not constitute a teaching of a layer of silicon dioxide the surface of which is doped with hydrogen ions by a plasma source ion implantation process as claimed. Nor would one conclude from reading Zhang or Nakanishi et al. that a doped layer of silicon dioxide as claimed would have a reduced level of sputtered metal contaminants when compared with a layer of silicon dioxide doped with hydrogen ions deposited by a Kauffman ion implantation process. The Examiner has failed to provide the required factual basis for anticipation.

Further, there is no teaching or evidence that if hydrogen ions existed in layer 104 of Zhang, such ions would be located in the surface of such a layer as claimed. While the Examiner asserts at page 13 that the surface would be inherently doped with hydrogen ions "because the hydrogen ions are substantially uniformly distributed in the layer of silicon dioxide," he has provided no evidence or reasoning to support his speculation.

Finally, claim 9 recites a doped layer of silicon dioxide; Zhang teaches formation a silicon oxynitride layer 104. Claim 9 recites a layer of polysilicon formed on the layer of silicon dioxide; Zhang teaches forming a layer of aluminum 105 over silicon oxynitride layer 104. While Zhang may suggest alternative compounds for use in layers 104 and 105, those alternatives are not preferred. And, in any event, one skilled in the art reading Zhang would be required to ignore Zhang's stated preferences, and to pick and choose among Zhang's possible alternatives, to arrive at the claimed device. Such a requirement for picking and choosing defeats any rejection for anticipation under §102. See, *In re Arkley*, *supra*.

Claim 10

Claim 10 is believed to be patentable over the cited references for at least the same reasons discussed above with respect to claim 9.

Further, claim 10 recites a “gate oxide formed on said semiconductor substrate from said layer of silicon dioxide having hydrogen ions implanted therein.” While the Examiner asserted at page 5 of the Office Action that Zhang shows “a gate oxide formed on the substrate from the layer of silicon dioxide,” he failed to identify where in Fig. 1 of Zhang such a “gate oxide” was located. That is because there is no gate oxide. Nowhere does Zhang teach such a gate oxide in the location recited in claim 10. Zhang does not anticipate claim 10 for this additional reason.

Rejection under 35 USC §102(b) as anticipated by Shufflebotham (US 5,711,998)

Claim 14

At page 7 of the final office action, the Examiner maintained his position that the limitation "having been doped with hydrogen ions deposited by a plasma source ion implantation process" does not structurally distinguish the claimed invention over the prior art. In addition, the Examiner maintained that substrate 301 of Shufflebotham inherently "has reduced sputtered metal contaminants in comparison with a substrate doped with ions deposited by a Kauffman ion implantation process." Applicant submits that claim 14 is patentable over Shufflebotham for the same reasons discussed above with regard to claim 9, namely that there is no teaching or suggestion in Shufflebotham of a layer of silicon dioxide the surface of which has been doped with hydrogen ions deposited by a plasma source implantation process. Rather, Shufflebotham teaches a method of hydrogenating polysilicon in an electrical device using a radio frequency high density plasma reactor.

With respect to Fig. 3 which the Examiner has relied upon, Shufflebotham states that during a typical hydrogenation process, hydrogen “diffuses through” the various layers of device 300 to reach and passivate the polysilicon in source 306A, drain 306B, channel 307, and gate 304. Nowhere does Shufflebotham describe a surface-doped semiconductor substrate layer as recited in claim 14. While the Examiner has asserted

that "at least some" hydrogen ions would inherently reach substrate 301 in Shufflebotham, he has provided no evidence to support such an assertion. And, proof of inherency requires proof that the asserted action will always and necessarily take place. The Examiner has not carried his evidentiary burden of proving inherency here. For these additional reasons, claim 14 is not anticipated by Shufflebotham.

Rejection under 35 USC §103(a) over Burns et al. (Principles of Electronic Circuits, pp. 380-381) in view of "Applicant's admitted prior art (APA)"

Claim 10

At page 8 of the final rejection, the Examiner acknowledged that Burns et al. do not teach the claimed layer of silicon dioxide having hydrogen ions implanted therein having reduced sputtered metal contaminants in comparison with a layer of silicon dioxide doped with ions deposited by a Kauffman ion implantation technique, but asserts that this teaching is inherent in the APA. However, how can something that is not taught by either reference be "inherent"? The answer is that it cannot. Burns is silent and the APA teaches using the Kauffman technique.

As discussed above with regard to claim 9, the APA does not teach that a silicon dioxide layer deposited with ions by a plasma ion source implantation process compared with that of the (same) silicon dioxide layer deposited with ions by a Kauffman ion implantation process would have reduced metal contaminants. The rejection is fundamentally flawed. It is not supported by evidence and should be reversed by this Board.

Claim 11

Claim 11 is believed to be patentable for the same reasons discussed above with regard to claim 10.

Claim 12

Claim 12 is believed to be patentable for the same reasons discussed above with regard to claim 10.

Rejection under 35 USC §103(a) over Murata et al. in view of "Applicant's admitted prior art (APA)"

Claim 14

The Examiner maintained at page 10 of the office action that it would have been obvious to combine Murata et al. with the "APA" based on his position that the "APA" inherently teaches a silicon dioxide layer having reduced sputtered metal contaminants in comparison with a layer doped with ions by a Kauffman ion implantation process, and that it would have been obvious to combine Murata et al. with the "APA." As pointed out above with regard to claim 9, how can something that is not taught by either reference be "inherent"? The answer is that it cannot. Murata is silent and the APA teaches using the Kauffman technique.

The APA does not teach that a silicon dioxide layer deposited with ions by a plasma ion source implantation process compared with that of the (same) silicon dioxide layer deposited with ions by a Kauffman ion implantation process would have reduced metal contaminants. Accordingly, the combined teachings of Murata et al. and the "APA" would not render claim 14 obvious. The Examiner's reasoning is fundamentally flawed, and the rejection should be reversed by this Board.

Conclusion

The claims are not anticipated by the cited prior art, which does not teach or suggest a layer of silicon dioxide formed on a semiconductor substrate having a surface with hydrogen ions deposited by a plasma source ion implantation process, where the layer of silicon dioxide has reduced sputtered metal contaminants in comparison with a layer of silicon dioxide doped with ions deposited by a Kauffman ion implantation process.

Further, the Examiner has failed to establish a prima facie case, by evidence or reasoning, that any of the rejected claims would have been obvious with respect to the proposed combination of references. None of the references teaches or suggests providing hydrogen ions implanted on the surface of a silicon dioxide substrate for the purpose of providing a subsequent layer of polycrystalline silicon which has a smooth morphology as claimed, where the layer of silicon dioxide has reduced sputtered metal contaminants in comparison with a layer of silicon dioxide doped with ions deposited by a Kauffman ion implantation process.

The Board is requested to reverse the rejections of claims 9-12 and 14 in their entirety.

Respectfully submitted,

DINSMORE & SHOHL LLP

By /Susan M. Luna/
Susan M. Luna
Registration No. 38,769

One Dayton Centre
One South Main Street, Suite 1300
Dayton, Ohio 45402-2023
Telephone: 937/449-6429
Facsimile: 937/449-6405

CLAIMS APPENDIX

9. A semiconductor device precursor comprising:

a semiconductor substrate;

a layer of silicon dioxide formed on said semiconductor substrate, the surface of said layer of silicon dioxide having been doped with hydrogen ions deposited by a plasma source ion implantation process, wherein said layer of silicon dioxide has reduced sputtered metal contaminants in comparison with a layer of silicon dioxide doped with ions deposited by a Kauffman ion implantation process; and

a layer of polycrystalline silicon formed on said layer of silicon dioxide, said layer of polycrystalline silicon having a smooth morphology.

10. A field effect transistor comprising:

a semiconductor substrate;

a layer of silicon dioxide formed on at least a portion of said semiconductor substrate, the surface of said layer of silicon dioxide having hydrogen ions implanted therein by plasma source ion implantation, wherein said layer of silicon dioxide has reduced sputtered metal contaminants in comparison with a layer of silicon dioxide doped with ions deposited by a Kauffman ion implantation process;

a layer of polycrystalline silicon formed on at least a portion of said layer of silicon dioxide, said layer of polycrystalline silicon having a smooth morphology; and

a gate oxide formed on said semiconductor substrate from said layer of silicon dioxide having hydrogen ions implanted therein by plasma source ion implantation;

a source and a drain formed in said semiconductor substrate with a gate electrode formed on said semiconductor substrate from said layer of polycrystalline silicon to form a field effect transistor.

11. A memory array comprising:

a semiconductor substrate;

a layer of silicon dioxide formed on at least a portion of said semiconductor substrate, wherein hydrogen ions are implanted into at least a portion of the surface of said layer of silicon dioxide by plasma source ion implantation, wherein said layer of silicon dioxide has reduced sputtered metal contaminants in comparison with a layer of silicon dioxide doped with ions deposited by a Kauffman ion implantation process;

a layer of polycrystalline silicon formed over at least said portion of said layer of silicon dioxide into which said hydrogen ions were implanted, said layer of polycrystalline silicon having a smooth morphology;

a plurality of memory cells arranged in rows and columns, each of said plurality of memory cells comprising at least one field effect transistor;

a gate oxide for each of said field effect transistors formed on said semiconductor substrate from said layer of silicon dioxide having hydrogen ions implanted therein by plasma source ion implantation;

a source and a drain for each of said field effect transistors formed in said semiconductor substrate; and

a gate electrode for each of said field effect transistors formed on said semiconductor substrate from said layer of polycrystalline silicon.

12. A semiconductor wafer comprising:

a wafer including a semiconductor substrate, said wafer being divided into a plurality of die;

a layer of silicon dioxide formed on at least a portion of said semiconductor substrate, on each of said plurality of die hydrogen ions are implanted into at least a portion of the surface of said layer of silicon dioxide by plasma source ion implantation, wherein said layer of silicon dioxide has reduced sputtered metal contaminants in comparison with a layer of silicon dioxide doped with ions deposited by a Kauffman ion implantation process;

a layer of polycrystalline silicon formed over at least said portion of said layer of silicon dioxide into which said hydrogen ions were implanted, said layer of polycrystalline silicon having a smooth morphology;

a repeating series of gate oxides formed on said semiconductor substrate from said layer of silicon dioxide having hydrogen ions implanted therein by plasma source ion implantation;

a repeating series of sources and drains for at least one field effect transistor formed on each of said plurality of die, said series of sources and drains being formed on said semiconductor substrate; and

a repeating series of gate electrodes for at least one field effect transistor formed on each of said plurality of die, said series of gate electrodes being formed on said semiconductor substrate from said layer of polycrystalline silicon.

14. A thin film transistor comprising:

a semiconductor substrate formed from a material selected from the group consisting of silicon dioxide, quartz and glass, the surface of said semiconductor substrate having hydrogen ions implanted therein by plasma source ion implantation, wherein said semiconductor substrate has reduced sputtered metal contaminants in comparison with a semiconductor substrate doped with ions deposited by a Kauffman ion implantation process;

a layer of polycrystalline silicon formed on at least a portion of said semiconductor substrate, said layer of polycrystalline silicon having a smooth morphology;

a layer of an insulating material formed on at least a portion of said layer of polycrystalline silicon;

a gate oxide formed from said layer of insulating material;

a source region and a drain region formed in said layer of polycrystalline silicon; and

a gate electrode formed on said layer of insulating material.

EVIDENCE APPENDIX

NONE

RELATED PROCEEDINGS APPENDIX

A related appeal was filed on December 19, 2005 (Appeal No. 2006-2669), and a decision was rendered in that appeal on September 21, 2007. A copy of the decision is attached hereto.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DAVID L. CHAPEK

Appeal 2006-2669
Application 09/605,293[1]
Technology Center 2800

Decided: September 21, 2007

Before ALLEN R. MACDONALD, JAY P. LUCAS,
and SCOTT R. BOALICK, *Administrative Patent Judges*.

BOALICK, *Administrative Patent Judge*.

DECISION ON APPEAL

This is an appeal under 35 U.S.C. § 134(a) from the rejection of claims 9-12 and 14, all the claims pending in the application. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

---

[1] Application filed June 28, 2000. The real party in interest is Micron Technology, Inc.

STATEMENT OF THE CASE

Appellant's invention relates to a semiconductor device having a layer of silicon dioxide that has been pretreated with hydrogen ions so that a polycrystalline film can be deposited smoothly and uniformly on the pretreated silicon dioxide layer. (Specification 1:1-3; 2:27 to 3:1.)

Claim 9 is exemplary:

9. A semiconductor device precursor comprising:

a semiconductor substrate;

a layer of silicon dioxide formed on said semiconductor substrate, the surface of said layer of silicon dioxide having been doped with hydrogen ions deposited by a plasma source ion implantation process, wherein said layer of silicon dioxide is free of sputtered metal contaminants; and

a layer of polycrystalline silicon formed on said layer of silicon dioxide, said layer of polycrystalline silicon having a smooth morphology.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Applicant's admitted prior art, pages 1-2 of the Specification under the heading "BACKGROUND OF THE INVENTION"

Murata	US 5,576,229	Nov. 19, 1996

Burns, Stanley G., "Principles of Electronic Circuits, pp. 177 and 308-381.

Claims 9-12 and 14 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite.

Claims 9 stands rejected under 35 U.S.C. § 102(a) as being anticipated by the Applicant's admitted prior art (AAPA).

Claims 10-12 stand rejected under 35 U.S.C. § 103(a) as being obvious over Burns and the AAPA.

Claim 14 stands rejected under 35 U.S.C. § 103(a) as being obvious over Murata and the AAPA.

Rather than repeat the arguments of Appellant or the Examiner, we make reference to the Briefs and the Answer for their respective details. Only those arguments actually made by Appellant have been considered in this decision. Arguments which Appellant could have made but chose not to make in the Briefs have not been considered and are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii) (2004).[2]

ISSUES

1. Whether Appellant has shown that the Examiner erred in rejecting claims 9-12 and 14 for indefiniteness under 35 U.S.C. § 112, second paragraph. The issue turns on whether one skilled in the art would understand the claim limitation "free of sputtered metal contaminants" when read in light of the specification.

---

[2] Except as will be noted in this opinion, Appellant has not presented any substantive arguments directed separately to the patentability of the dependent claims or related claims in each group. In the absence of a separate argument with respect to those claims, they stand or fall with the representative independent claim. *See* 37 C.F.R. § 41.37(c)(1)(vii).

2. Whether Appellant has shown that the Examiner erred in rejecting claim 9 under 35 U.S.C. § 102(a). The issue turns on whether the AAPA teaches or discloses each and every limitation of claim 9.

3. Whether Appellant has shown that the Examiner erred in rejecting claims 10-12 under 35 U.S.C. § 103(a). The issue turns on whether the AAPA and Burns teach or disclose the claimed subject matter.

4. Whether Appellant has shown that the Examiner erred in rejecting claim 14 under 35 U.S.C. § 103(a). The issue turns on whether the AAPA and Murata teach or disclose the claimed subject matter.

FINDINGS OF FACT

The record supports the following findings of fact (FF) by a preponderance of the evidence.

1. Appellant describes semiconductor devices that are made using a method for pre-treating a silicon dioxide film with hydrogen ions that provides a subsequently deposited polycrystalline silicon film with a smooth morphology. (Specification Abstract; 1:1-3.) In particular, the method involves using a plasma source ion implantation (PSII) technique to pre-treat the silicon dioxide film with hydrogen ions. (Specification 8:16 to 9:16.)

2. In the "Background of the Invention" section, the Specification states that:

> Currently in the art, silicon dioxide films are pretreated with hydrogen ions to prepare the surface of the silicon dioxide film for the deposition of a layer of polycrystalline silicon to provide for a thinner and smoother polycrystalline silicon film. The silicon dioxide is pretreated by ion beam bombardment by a Kaufman ion source. Hydrogen ion beam pretreatment is typically performed using a Kaufman ion beam source directed normally to the substrate. A Kaufman ion source employs a metal grid to accelerate ions at a particular target. During an ion implantation process using a Kaufman ion source, metal from the metal grid sputters off of the grid and becomes implanted in the target object causing the target object to become contaminated. As the size of devices on the target object decreases, the effect of damage caused by sputtered metal from the metal grid increases.

(Specification 1:12-22.)

3. The Specification also states that:

> Unlike a Kaufman ion source implantation technique, a plasma source ion implantation apparatus does not employ a metal grid to accelerate the hydrogen ions toward the target object but instead uses the target object itself, in this case the substrate 12, to accelerate the ions toward the target object. Thus, plasma source ion implantation reduces the possibility of contamination of the target object by eliminating a device which employs a metal grid. Further, plasma source ion implantation can be used on smaller devices or substrates than a Kaufman ion

> source without increasing the likelihood for contamination of the target object.

(Specification 10:6-13.)

PRINCIPLES OF LAW

On appeal, all timely filed evidence and properly presented argument is considered by the Board. *See In re Piasecki*, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984).

In the examination of a patent application, the Examiner bears the initial burden of showing a prima facie case of unpatentability. *Id.* at 1472, 223 USPQ at 788. When that burden is met, the burden then shifts to the applicant to rebut. *Id.*; *see also In re Harris*, 409 F.3d 1339, 1343-44, 74 USPQ2d 1951, 1954-55 (Fed. Cir. 2005) (finding rebuttal evidence unpersuasive). If the applicant produces rebuttal evidence of adequate weight, the prima facie case of unpatentability is dissipated. *In re Piasecki*, 745 F.2d at 1472, 223 USPQ at 788. Thereafter, patentability is determined in view of the entire record. *Id.* However, on appeal to the Board it is an appellant's burden to establish that the Examiner did not sustain the necessary burden and to show that the Examiner erred -- on appeal we will not start with a presumption that the Examiner is wrong.

The purpose of the second paragraph of 35 U.S.C. § 112 "is to provide those who would endeavor, in future enterprise, to approach the area circumscribed by the claims of a patent, with the adequate notice demanded by due process of law, so that they may more readily and accurately determine the boundaries of protection involved and evaluate the possibility of infringement and dominance." *In re Hammack*, 427 F.2d 1378, 1382, 166

USPQ 204, 208 (CCPA 1970). The test for definiteness under the second paragraph of 35 U.S.C. § 112 is "whether those skilled in the art would understand what is claimed when the claim is read in light of the specification." *Orthokinetics, Inc. v. Safety Travel Chairs, Inc.*, 806 F.2d 1565, 1576, 1 USPQ2d 1081, 1088 (Fed. Cir. 1986).

Anticipation is established when a single prior art reference discloses expressly or under the principles of inherency each and every limitation of the claimed invention. *Atlas Powder Co. v. IRECO Inc.*, 190 F.3d 1342, 1347, 51 USPQ2d 1943, 1946 (Fed. Cir. 1999); *In re Paulsen*, 30 F.3d 1475, 1478-79, 31 USPQ2d 1671, 1673 (Fed. Cir. 1994).

"Section 103 forbids issuance of a patent when 'the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.'" *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1734, 82 USPQ2d 1385, 1391 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, and (3) the level of skill in the art. *Graham v. John Deere Co.*, 383 U.S. 1, 17-18, 148 USPQ 459, 467 (1966). *See also KSR*, 127 S. Ct. at 1734, 82 USPQ2d at 1391 ("While the sequence of these questions might be reordered in any particular case, the [*Graham*] factors continue to define the inquiry that controls."). The Court in *Graham* further noted that evidence of secondary considerations, such as commercial success, long felt but unsolved needs, failure of others, etc., "might be

utilized to give light to the circumstances surrounding the origin of the subject matter sought to be patented." 383 U.S. at 18, 148 USPQ at 467.

During examination of patent application, a claim is given its broadest reasonable construction consistent with the specification. *In re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-51 (CCPA 1969). "[T]he words of a claim 'are generally given their ordinary and customary meaning.'" *Phillips v. AWH Corp.,* 415 F.3d 1303, 1312, 75 USPQ2d 1321, 1326 (Fed. Cir. 2005) (en banc) (internal citations omitted). The "ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application." *Id.* at 1313, 75 USPQ2d at 1326.

A product-by-process claim enables "an applicant to claim an otherwise patentable product that resists definition by other than the process by which it is made." *In re Thorpe*, 777 F.2d 695, 697, 227 USPQ 964, 966 (Fed. Cir. 1985). "To the extent these process limitations distinguish the *product* over the prior art, they must be given the same consideration as traditional product characteristics." *In re Luck*, 476 F.2d 650, 653, 177 USPQ 523, 525 (CCPA 1973).

"[E]ven though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself." *Id.* In other words, "once a product is fully disclosed in the art, future claims to that same product are precluded, even if that product is claimed as made by a new process." *Smithkline Beecham Corp. v. Apotex Corp.*, 439 F.3d 1312, 1315, 78 USPQ2d 1097, 1099 (Fed. Cir. 2006).

"Where a product-by-process claim is rejected over a prior art product that appears to be identical, although produced by a different process, the burden is upon the applicants to come forward with evidence establishing an unobvious difference between the claimed product and the prior art product." *In re Marosi*, 710 F.2d 799, 803, 218 USPQ 289, 292-93 (Fed. Cir. 1983).

ANALYSIS

Appellant contends that Examiner erred in rejecting claims 9-12 and 14. Reviewing the documents of record and the findings of facts cited above, we do not agree that the Examiner erred in rejecting claims 9-12 and 14 as being indefinite. However, we agree with Appellant that the Examiner erred in rejecting claim 9 as being anticipated by the AAPA, claims 10-12 as being obvious over Burns and the AAPA, and claim 14 as being obvious over Murata and the AAPA.

Issue 1: Indefiniteness Rejection of Claims 9-12 and 14

The Examiner found that the recited limitation of a silicon dioxide layer (claims 9-12) or a semiconductor substrate (claim 14) "free of sputtered metal contaminants" rendered the claims indefinite. (Answer 5.) Appellant argues that the Examiner erred in finding claims 9-12 and 14 indefinite because:

> the specification clearly describes the problem of sputtered metal contaminants resulting from the use of a Kaufmann ion source which includes a metal grid (see page 1), and teaches that using PSII reduces metal contamination because it eliminates the use of a metal grid (page 10). In light of this

> teaching in the specification, it is submitted that one of ordinary skill in the art would understand that the limitation "free of sputtered metal contaminants" means that the layer of silicon dioxide has no sputtered metal contaminants present.

(Reply Br. 2; *see also* Br. 5-6.) Appellant contends that the claim term "free of sputtered metal contaminants" does not require that the layer (or substrate in claim 14) be free from all metal contaminants, just *sputtered* metal contaminants. (Br. 6.)

We agree with the Examiner that the limitation "free of sputtered metal contaminants" renders claims 9-12 and 14 indefinite. (Answer 5, 10-12.) The Examiner found that "free" is a relative term "because accepted physics principles dictate that no material will be completely free of metal contaminants." (Answer 5.) Therefore, the Examiner found that "in the context of the claims, one of ordinary skill in the art would not know what level of contaminants is required to meet the limitation." (Answer 5.) We agree with the Examiner that the Specification "does not define any standard for determining the level of contaminants present" and "does not provide any objective standard for the relative term such that one of ordinary skill in the art would not know what level of contaminants is needed to be considered 'free.'" (Answer 5.)

We agree with the Examiner that "Appellant merely points out that their process eliminates one specific source of sputtered metal contaminants (the metal grid in the Kaufman ion source)" so as to reduce but not eliminate the possibility of sputtered metal contamination. (Answer 10.) We also agree with the Examiner that Appellant's reliance on *In re Marosi*, 710 F.2d

199, 218 USPQ 289 (Fed. Cir. 1983) is misplaced. (Answer 11.) The *Marosi* court found that the claim limitation "essentially free of alkali metal" was not indefinite because the specification provided a general guideline and examples sufficient to enable a person of ordinary skill in the art to draw a line between unavoidable impurities in starting materials and essential ingredients. *Id.* at 803, 218 USPQ at 292. Unlike *Marosi*, the instant Specification provides no general guideline or examples sufficient to enable a person of ordinary skill in the art to draw a line and determine if the limitation "free of sputtered metal contaminants" is satisfied.

In addition, the Examiner found that there would be no difference between the structure of a sputtered metal contaminant and the structure of other metal contaminants in the devices claimed by claims 9-12 and 14. (Answer 12.) Therefore, the Examiner found that a person of ordinary skill in the art would not be able to determine whether a contaminant in the claimed devices "was sputtered or introduced in another way." (Answer 12.)

Appellant has not come forward with evidence to rebut the Examiner's findings. Appellant merely alleges that, in light of the teachings in the Specification regarding Kaufman ion sources and PSII (*see* FF 2-3), one of ordinary skill would understand that the limitation "free of sputtered metal contaminants" means that no sputtered metal contaminants are present. (Reply Br. 2.) However, "[a]rgument in the brief does not take the place of evidence in the record." *In re Schulze*, 346 F.2d 600, 602, 145 USPQ 716, 718 (CCPA 1965) (citing *In re Cole*, 326 F.2d 769, 773, 140 USPQ 230, 233 (CCPA 1964)).

Therefore, we conclude that the Examiner did not err in rejecting claims 9-12 and 14 as indefinite under 35 U.S.C. § 112, second paragraph.

Issue 2: Anticipation Rejection of Claim 9

The Examiner found that "[t]he admitted prior art does not explicitly state the layer of silicon dioxide being 'free of sputtered metal contaminants' but this limitation is considered implicitly understood." (Answer 6.) The Examiner interpreted the limitation "free of sputtered metal contaminants" to mean "sufficiently free so as to operate." (Answer 6-7.) Therefore, the Examiner found that claim 9 was written broadly enough to read on a conventional layer of silicon dioxide treated with hydrogen ions using a Kaufman ion source. (Answer 7; 13.) In addition, the Examiner found that "[s]ince the claims are drawn to a product, the process by which the contamination is introduced is immaterial since the final structure of a metal contaminant is the same regardless of how it got there. Thus, any number of metal contaminants is encompassed by the claimed device." (Answer 14.)

Appellant argues that the limitation "free of sputtered metal contaminants" should not be interpreted "as encompassing a layer which *includes* sputter [sic, sputtered] metal contaminants as a result of treatment with a Kaufman ion source as described in 'Applicant's admitted prior art.'" (Reply Br. 3; *see also* Br. 7.) We agree.

The Specification teaches that the use of a Kaufman source results in metal sputtering off the metal grid and contaminating the target object. (FF 2.) Therefore, it is not consistent with the Specification to interpret the claim limitation "free of sputtered metal contaminants" in such a way that enables it to be met by a silicon dioxide layer (or semiconductor substrate) that explicitly encompasses sputtered metal contaminants introduced through the use of a Kaufman source.

Therefore, we conclude that the Examiner erred in rejecting claim 9 as anticipated by the AAPA.

Issues 3 & 4: Obviousness Rejections of Claims 10-12 and 14

In rejecting claims 10-12 and 14, the Examiner relied on the AAPA for a teaching of a layer of silicon dioxide (or a semiconductor substrate in claim 14) that is "free of sputtered metal contaminants." (Answer 7-10, 15, and 17.) However, as discussed with respect to claim 9, it is not consistent with the Specification to interpret the claim limitation "free of sputtered metal contaminants" in such a way that enables it to be met by a silicon dioxide layer (or semiconductor substrate) that explicitly encompasses sputtered metal contaminants introduced through the use of a Kaufman source.

Therefore, we conclude that the Examiner erred in rejecting claims 10-12 as being obvious over AAPA and Burns and erred in rejecting claim 14 as being obvious over AAPA and Murata.

NEW GROUNDS OF REJECTION UNDER 37 C.F.R. § 41.50(b)

We make the following new grounds of rejection using our authority under 37 C.F.R. § 41.50(b).

35 U.S.C. § 112, First Paragraph

Claims 9-12 and 14 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. The claims contain subject matter which was not described in the Specification in such a way as to reasonably convey to one skilled in the

relevant art that the inventor, at the time the application was filed, had possession of the claimed invention.

Claims 9-12 and 14 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. The claims contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claims 9-12 recite the limitation "wherein said layer of silicon dioxide is free of sputtered metal contaminants" and claim 14 recites the limitation "wherein said semiconductor substrate is free of sputtered metal contaminants." These limitations were added by amendment after the filing date of the instant Specification.

The Specification provides no special meaning for the claim term "free of sputtered metal contaminants."[3] The plain meaning of the claim term "free of" is "lacking; without." *Webster's New World Dictionary Third College Edition* 537 (1994). The originally-filed Specification does not teach or describe a device that is lacking or without sputtered metal contaminants. Instead, the Specification describes a semiconductor device made by a process that *reduces* the possibility of contamination when compared to the prior art Kaufman ion source implantation technique. (FF 3.) In particular, the Specification teaches that the possibility of contamination is reduced because the metal grid used by the Kaufman ion source technique is not present. (FF 3.) The Specification also teaches that the process used to make the device can be used on smaller devices than a Kaufman ion source *without increasing* the likelihood of contamination.

---

[3] Indeed, the Specification never uses the term "free of."

(FF 3) In other words, the Specification teaches a device where the possibility of sputtered metal contamination is *reduced*, not *eliminated*. Although the Specification teaches removal of one source of sputtered metal contamination to reduce the possibility of contamination, the Specification does not teach removal of all possible sources of sputtered metal contamination. The originally-filed Specification simply contains no teaching or description of a device free of (i.e., without any) sputtered metal contaminants.

Accordingly, the originally-filed Specification lacks both written description and enablement for the limitation "wherein said layer of silicon dioxide is free of sputtered metal contaminants" recited by claims 9-12 and for the limitation "wherein said semiconductor substrate is free of sputtered metal contaminants" recited by claim 14.

This decision contains new grounds of rejection pursuant to 37 C.F.R. § 41.50(b) (effective September 13, 2004, 69 Fed. Reg. 49960 (August 12, 2004), 1286 Off. Gaz. Pat. Office 21 (September 7, 2004)).

37 C.F.R. § 41.50(b) provides that, "new ground[s] of rejection pursuant to this paragraph shall not be considered final for judicial review."

37 C.F.R. § 41.50(b) also provides that the Appellants, *WITHIN TWO MONTHS FROM THE DATE OF THE DECISION*, must exercise one of the following two options with respect to the new grounds of rejection to avoid termination of proceedings (37 C.F.R. § 1.197 (b)) as to the rejected claims:

(1) Reopen prosecution. Submit an appropriate amendment of the claims so rejected or new evidence relating to the claims so rejected,

> or both, and have the matter reconsidered by the examiner, in which event the proceeding will be remanded to the examiner …
>
> (2) Request rehearing. Request that the proceeding be reheard under 37 C.F.R. § 41.52 by the Board upon the same record …

CONCLUSION OF LAW

Based on the findings of facts and analysis above, we conclude that:

(1) The Examiner did not err in rejecting claims 9-12 and 14 for indefiniteness under 35 U.S.C. § 112, second paragraph.

(2) The Examiner erred in rejecting claim 9 for anticipation under 35 U.S.C. § 102(a).

(3) The Examiner erred in rejecting claims 10-12 for obviousness under 35 U.S.C. § 103.

(4) The Examiner erred in rejecting claim 14 for obviousness under 35 U.S.C. § 103.

(5) Claims 9-12 and 14 are unpatentable under 35 U.S.C. § 112, first paragraph, because they fail to comply with the written description requirement.

(6) Claims 9-12 and 14 are unpatentable under 35 U.S.C. § 112, first paragraph, because they fail to comply with the enablement requirement.

DECISION

The rejection of claims 9-12 and 14 for indefiniteness under 35 U.S.C. § 112, second paragraph, is affirmed.

The rejection of claim 9 for anticipation under 35 U.S.C. § 102(a) is reversed.

The rejection of claim 10-12 for obviousness under 35 U.S.C. § 103 is reversed.

The rejection of claim 14 for obviousness under 35 U.S.C. § 103 is reversed.

Claims 9-12 and 14 are rejected for failure to comply with the written description requirement of 35 U.S.C. § 112, first paragraph.

Claims 9-12 and 14 are rejected for failure to comply with the enablement requirement of 35 U.S.C. § 112, first paragraph.

New grounds of rejection have been entered under 37 C.F.R. § 41.50(b).

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

<u>AFFIRMED</u>
<u>37 C.F.R. § 41.50(b)</u>

pgc

Dinsmore & Shohl LLP
One Dayton Centre, One South Main Street
Suite 1300
Dayton, OH 45402-2023